MULTIPLEXING- AND DEMULTIPLEXING-TECHNIQUES WITH GUNN DEVICES IN THE GBIT/S RANGE

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Abstract

In this paper a circuit is described which can process signals in the Gbit/s range for a fast PCM technique. A shift register with Gunn devices monolithically integrated on GaAs is used. A 4-stage arrangement is described. Experimental results for a bitrate of 1.8 Gbit/s are reported.

Introduction

To process signals in a PCM technique in the Gbit/s range multiplexing and demultiplexing systems are needed. Important components of such systems are fast shift registers. This paper describes a dynamic shift register as an example of circuit integration with Gunn devices the technique of which offers advantages in the Gbit/s range. The complex performance of Gunn devices carrying high-field domains makes possible a variety of logic operations which can be carried out in one device.[1,2] Further merits are the steep ramps of the pulses generated[3,4], the small delay between subsequent stages[4], and the automatic regeneration of the pulse shape within the circuit. In most cases these properties of Gunn devices result in a considerable simplification of the circuit design as compared to circuits with bipolar transistors or field-effect transistors. Additionally planar devices on semi-insulating GaAs substrate show good insolation against each other so that the mutual interaction through parasitic effects being the speed determining factor in this range[5] remains small.

Principle of circuit

The main component of the multiplexing system is a monolithically integrated, dynamic shift register with Gunn devices the principle of which is depicted in Fig. 1. The register consist of a chain of regenerative AND gates, each followed by a delay structure. AND gates can be realized by two Schottky gates side by side on the channel of a planar Gunn device just in front of the cathode contact.[1] Fig. 2 shows a microphotograph of such a Gunn device in an integrated circuit. The delay of the signal is determined by the time needed by the domains to run from the trigger gates to a narrow capacitive electrode adjacent to the anode. The potential of the channel under this electrode is changed when the domain passes under the electrode. Consequently a negative pulse is generated at the electrode which can be utilized[6] to trigger the following Gunn device.

The delay time t_d per stage of the register obtained in such a way naturally is shorter than the domain transit time or the current-pulse width t_p generated by the domain. Therefore two delay sections are needed for the duration of one bit. According to Fig. 1 it is advantageous to employ as a clock two sinusoidal voltages of the period t_c, shifted against each other by half the width of a bit. These voltages are connected to the input terminals of succeeding stages. The condition $t_c = 2\,t_d > t_p$ must be fulfilled.

Fig. 3 gives the circuit of a complete demultiplexing arrangement. The register consists of four cells with eight Gunn devices of the kind depicted in Fig. 2. Four additional Gunn devices operate as AND gates in the read-out circuit. These latter Gunn devices are activated during the fourth bit thereby switching the information contained in the shift register to the parallel output terminals. The clock voltage for the gate circuit is generated from the sinusoidal voltage of frequency $f_c = 1/t_c$ applied to the register. Gunn devices, operating as frequency deviders, can be used for this purpose.[7] Furthermore the pulse width is stretched in the read-out circuit so that transistor circuits can be controlled. The pulse-width stretching is effectively achieved by simply choosing an adequately long channel for the Gunn devices in the read-out circuit.

Circuit design and experimental results

A section of the monolithically integrated shift register with four Gunn devices is given in Fig. 4. The devices are of a mesa structure etched from an epitaxial layer of about 1 µm in thickness and of a carrier concentration of 3×10^{16} cm^{-3}. The whole circuit is protected with a sputtered SiO_2 film about 0.2 µm thick with the exception of the areas for the Schottky gates and of the connection areas of the lines conducted in two planes. The channel length equivalent to the delay time is 27 µm. With the domain velocity of 1×10^{7} cm/s a bit rate of 1.8 Gbit/s is derived. The bias voltage for the trigger gates is applied through the meandering resistors. The time constant $\tau_G = R_G C_G$ of the gate circuit must fulfill the requirement $t_r \leq \tau_G \ll t_{tr}$ (t_r domain growth time; t_{tr} domain transit time; R_G and C_G resistance and total capacity of the gate circuit, resp.) so that the domain is safely triggered and that the gate circuit can be discharged within the domain transit time. For the circuit described here the following data are typical: $t_{tr} \approx 350$ ps; $t_r \approx 50$ ps; $C_G \approx 30$ fF; $\tau_G \approx 100$ ps.

The electrical performance of the circuit becomes clear from Figs. 5 and 6. The time variation of the currents i_1 to i_4 and i_1 to i_3, respectively, for subsequent stages are depicted. The mode of operation of Fig. 5 is equivalent to a series-parallel transformation. A pulse sequence ...001100... of 1.8 Gbit/s is applied to the series input terminal. As can be seen from the time variation of the currents i_1 to i_4 the pulse sequence moves through the register with a delay

t_d = 275 ps per stage. After the time 4 t_d = 1.1 ns the two "1"-bits of the input signal appear simultaneously on the first and second parallel output terminal (i_2 and i_4: cf. Fig. 3). Thus the 1.8 Gbit/s data stream is converted into two parallel data streams of 900 Mbit/s each.

The reverse conversion is demonstrated with a simular circuit (Fig. 6). The first and third stage of the register are triggered simultaneously with a pulse sequence of ...0010100... at a rate of 1.7 Gbit/s. This pulse sequence is generated from the sequence ...001100... with half the bit rate employing a gate circuit. The pulse sequence corresponding to the time variation i_1 is added to the initial sequence i_3 after the former passed two delay sections. This results in the sequence ...00111100... at 1.7 Gbit/s. Thus the circuit converts two data streams of 850 Mbit/s each into a data stream of 1.7 Gbit/s.

The integrated circuits described here process NRZ and RZ signals at the input terminal equally well which is a consequence of the clocked AND gates employed. The power consumption under CW condition is approximately 250 mW per stage. Up to five stages were monolithically integrated on an area of 750x150 μm^2. Simple cooling precautions were sufficient to derive the heat through the 250 μm thick GaAs substrate.

Conclusion

Monolithic circuit integration on GaAs can be used to advantage in a multiplexing technique in the subnanosecond range. Planar Gunn devices which due to their complex performance make possible a variety of logic functions are employed as active components. A shift register is described which performs the logic AND operation and the pulse delay in one Gunn device per stage. The pulse delay is realized as the transit time of a domain in the channel of the Gunn device. A shift register was fabricated the Gunn devices of which act as delay sections of about 30 μm. First experimental results prove the suitability of the circuit for multiplexing and demultiplexing operation at approximately 1.8 Gbit/s. Provided that the dimensions of the circuit are decreased it can be expected that some Gbit/s can be processed.

Literature

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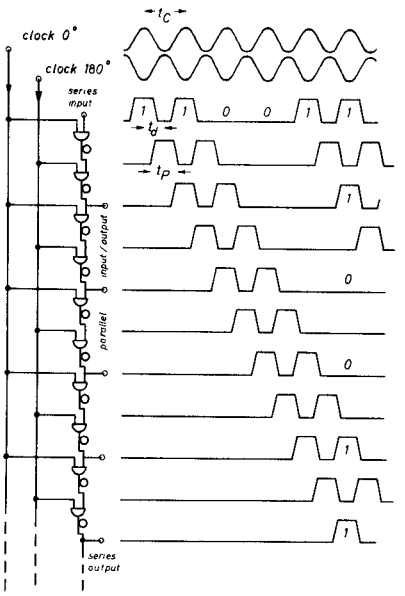

Fig. 1. Principle of a dynamic shift register composed from AND gates and delay structures. The pulse pattern is shown for the case of a series-to-parallel transformation.

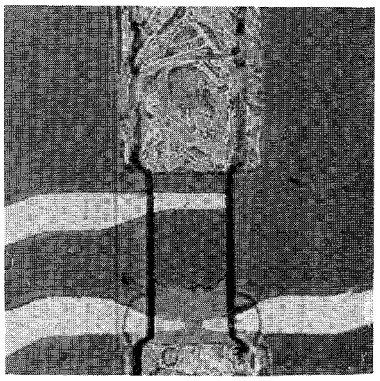

Fig. 2. Active component of the register. The planar Gunn device performs an AND operation with the Schottky gates in front of the cathode and causes a signal delay by coupling the signal to the capacitive electrode adjacent to the anode.

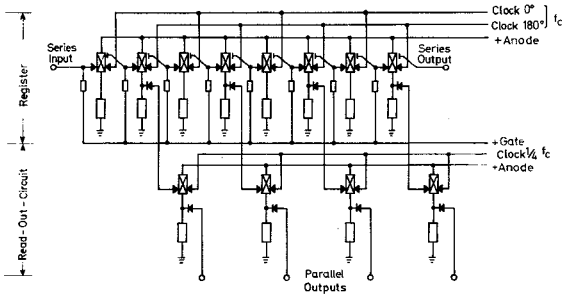

Fig. 3. Demultiplexing circuit with Gunn devices. The register consists of four cells with two Gunn devices each after Fig. 2. Four additional Gunn devices operating as AND gates serve for parallel reading-out of the information stored in the register.

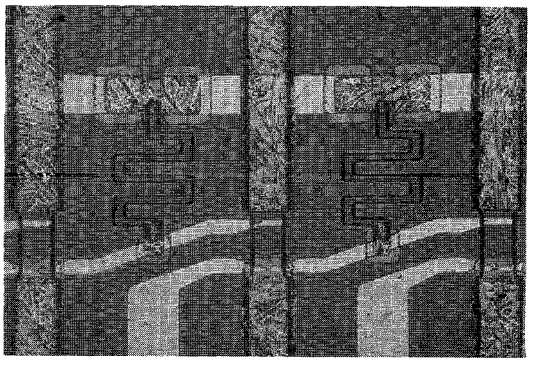

Fig. 4. Section of a monolithically integrated circuit of a shift register. The essential parts of the circuit are Gunn devices, meandering resistors in the gate circuit, and metallic connection lines. The lines are arranged in two planes. SiO_2 serves as an insolating film.

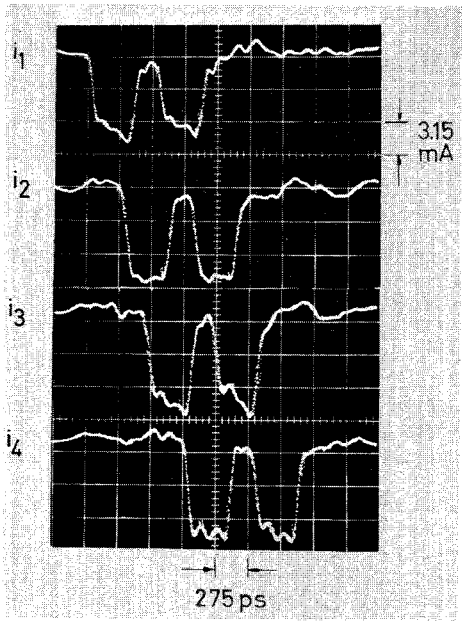

Fig. 5. Electrical performance of the shift register in the series-to-parallel conversion mode. The time variation of the currents i_1 to i_4 through four stages succeeding each other is shown under the condition that a pulse sequence ...001100... at 1.8 Gbit/s is applied to the series input terminal.

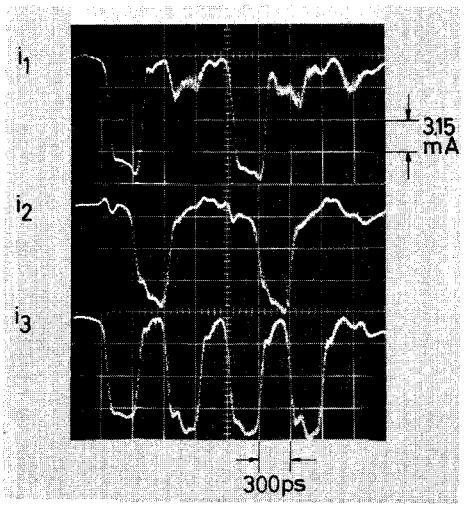

Fig. 6. Electrical performance of the shift register in the parallel-to-series conversion mode. The time variation of the currents i_1 to i_3 through three stages is depicted. The pulse sequence ...0010100... at 1.7 Gbit/s is applied simultaneously to the first and second parallel input terminal (first and third stage of the register).